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IN THE CLAIMS

Please amend claims 4, 11-12, 15, 19, 21-22, 25-26, 29, 31, and 33 as follows:

1. (Previously Presented) An apparatus for spreading electromagnetic interference associated with an electrical system over a range of frequencies, the electrical system having a pulse width modulator that provides a clock signal and having a power source connected to the pulse width modulator, the apparatus comprising:

a binary counter having a clock input and a plurality of outputs, wherein the clock signal is operatively coupled to the clock input;

a plurality of resistors, wherein each of the resistors is coupled between a different one of the plurality of outputs of the binary counter and a node;

a timing resistor coupled between a first voltage potential and the node;

a timing capacitor coupled between the node and a second voltage potential; and

wherein the node is coupled to an input of the pulse width modulator.

2. (Original) The apparatus of claim 1, wherein the binary counter is a unidirectional counter.

3. (Original) The apparatus of claim 1, wherein the binary counter is an up/down counter.

4. (Currently Amended) The apparatus of claim 1, wherein each of the plurality of ~~parallel~~ resistors is binary weighed and includes a base value and a multiplier value.

5. (Previously Presented) The apparatus of claim 4, wherein the base value is between approximately 100 kilohms and 1000 kilohms.

6. (Previously Presented) The apparatus of claim 1, wherein the timing resistor has a value between approximately 1.0 kilohms and 10.0 kilohms.

7. (Previously Presented) The apparatus of claim 1, wherein the timing capacitor has a value in the range of approximately 0.1 nanofarrrads and 10.0 nanofarrads.

8. (Previously Presented) The apparatus of claim 1, further comprising:

a resistor divider network comprising:

a first resistor connected to the clock signal of the pulse width modulator;

a second resistor connected between the first resistor and a third voltage; and

wherein the clock input of the binary counter is operatively coupled between the first and the second resistors.

9. (Previously Presented) The apparatus of claim 8, wherein the first and second resistors each have a value between approximately 1.0 kilohms and 50.0 kilohms.

10. (Previously Presented) An apparatus creating a pulse train signal of a pulse width modulator whose fundamental frequency is time-varying, the apparatus comprising:

a power source coupled to the pulse width modulator;

a resistor/capacitor network coupled to the pulse width modulator, the resistor/capacitor network having a resistor/capacitor time constant;

incrementing means for incrementing a binary count; and

altering means coupled between the incrementing means and the resistor/capacitor network for altering the resistor/capacitor time constant based on the binary count to correspondingly time-vary the fundamental frequency of the pulse train signal of the pulse width modulator.

11. (Currently Amended) The apparatus of claim 10, wherein the altering means ~~further~~ comprise:

a plurality of resistors, wherein each of the resistors is coupled between a corresponding different output of a binary counter and a first voltage potential.

12. (Currently Amended) A system comprising:

a power source;

a pulse width modulator coupled to the power source, the pulse width modulator providing a pulse train signal at an output;

a binary counter coupled to the pulse width modulator, the binary counter having an input and a plurality of outputs, wherein the pulse train signal is operatively coupled to the input;

a plurality of resistors, wherein each of the resistors is operatively coupled between a corresponding different one of the pluarality of outputs of the binary counter and operatively coupled to a node;

a timing resistor operatively coupled between a first voltage potential and the node;

a timing capacitor operatively coupled between the node and a second voltage potential; and

wherein the node is operatively coupled to an input of the pulse width ~~generator~~modulator.

13. (Original) The system of claim 12, wherein the binary counter is a unidirectional counter.

14. (Original) The system of claim 12, wherein the binary counter is an up/down counter.

15. (Currently Amended) The system of claim 12, wherein each of the plurality of ~~parallel~~ resistors is binary weighted and includes a base value and a multiplier value.

16. (Previously Presented) The system of claim 15, wherein the base value is between approximately 100 kilohms and 1000 kilohms.

17. (Previously Presented) The system of claim 12, wherein the timing resistor has a value between approximately 1.0 kilohms and 10.0 kilohms.

18. (Previously Presented) The system of claim 12, wherein the timing capacitor has a value between approximately 0.1 nanofarrads and 10.0 nanofarrads.

19. (Currently Amended) The system of claim 12, further comprising:

a resistor divider network operatively coupled between the pulse width modulator and the binary counter, the resistor divider network ~~further~~ comprising:

a first resistor connected to the ~~clock signal~~output of the pulse width ~~generator~~modulator;

a second resistor connected between the first resistor and a third voltage potential; and

wherein the ~~clock~~ input of the binary counter is operatively coupled between the first and the second resistors.

20. (Previously Presented) The system of claim 19, wherein the first and second resistors each have a value between approximately 1.0 kilohms and 50.0 kilohms.

21. (Currently Amended) The system of claim 12, further comprising:

a resistor divider network coupled between the output of the pulse width modulator and ~~an~~ the input of the binary counter.

22. (Currently Amended) A system for disposing electromagnetic interference associated with a DC-DC converter, the system comprising:

a power switch for receiving an input power;

a filter operatively coupled to the power switch;

a pulse width modulator clock control stage operatively coupled to the power switch, the pulse width modulator clock control stage ~~further~~ comprising:

a power source;

a pulse width modulator coupled to a pulse train source, the pulse width modulator providing a pulse train signal at an output;

a binary counter coupled to the pulse width modulator, the binary counter having an input and a plurality of outputs, wherein the pulse train signal at the output of the pulse width modulator is operatively coupled to the input of the binary counter;

a plurality of resistors, wherein each of the resistors is operatively coupled between a corresponding different one of the outputs of the binary counter and operatively coupled to a node;

a timing resistor operatively coupled between a first voltage potential and the node;

a timing capacitor operatively coupled between the node and a second voltage potential; and

wherein the node is coupled to an input of the pulse width ~~generator~~modulator.

23. (Original) The system of claim 22, wherein the binary counter is a unidirectional counter.

24. (Original) The system of claim 22, wherein the binary counter is an up/down counter.

25. (Currently Amended) The system of claim 22, wherein each of the plurality of ~~parallel~~ resistors is binary weighted and includes a base value and a multiplier value.

26. (Currently Amended) The system of claim ~~22~~25, wherein the base value is between approximately 100 kilohms and 1000 kilohms.

27. (Previously Presented) The system of claim 22, wherein the timing resistor has a value between approximately 1.0 kilohms and 10.0 kilohms.

28. (Original) The system of claim 22, wherein the timing capacitor has a value between approximately 0.1 and 10.0 nanofarrads.

29. (Currently Amended) The system of claim 22, ~~further~~ further comprising:

a resistor divider network operatively coupled between the pulse width modulator and the binary counter, the resistor divider network ~~further~~ comprising:

a first resistor connected to the ~~clock signal~~output of the pulse width ~~generator~~modulator;

a second resistor connected between the first resistor and a third voltage potential; and

wherein the ~~clock~~ input of the binary counter is operatively coupled between the first and the second resistors.

30. (Previously Presented) The system of claim 29, wherein the first and second resistors of the resistor divider network each have a value between approximately 1.0 kilohms and 50.0 kilohms.

31. (Currently Amended) A method of creating a pulse train signal of a pulse width modulator having a fundamental frequency that is time-varying, the method comprising:

incrementing a binary count;

altering a resistor/capacitor time constant of a resistor/capacitor network based upon the binary count; and

creating the pulse train signal of the pulse width modulator having ~~a~~ the fundamental frequency that is time-varying, ~~whose~~ wherein the fundamental frequency of the pulse train signal is based upon the resistor/capacitor time constant.

32. (Original) The method of claim 31, wherein the step of altering ~~a~~ the resistor/capacitor time constant ~~further~~ comprises:

operatively coupling a plurality of resistors to ~~an~~ a respective output of a binary counter.

33. (Currently Amended) The method of claim 31, wherein the step of incrementing ~~a~~ the binary count ~~further~~ comprises:

incrementing ~~a~~ the binary count of a binary counter by coupling the pulse train signal from the pulse width modulator to an input of the binary counter.